REMARKS

In the Office Action, claims 1-7 were objected to. Claims 1-7 were rejected under 35 USC §102(b) as being anticipated by Takiar et al.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "Version With Markings To Show Changes Made".

Takiar et al. was cited as showing the general prior art in the International Search report. The Takiar patent relies entirely on wire-bonded connections and ordinary integrated circuit packages and hence cannot be regarded as particularly relevant to the present invention.

The Takiar patent is only relevant in the respect that it discloses stacked circuit modules, e.g. as apparent from any of the figs. 3,4,5 and 6 thereof. Contact pads, e.g. 94, 96, 98 as shown in fig. 3 of the Takiar patent is located on the upper and exposed surfaces of the circuit chips 74, 76, 78 respectively. The circuit chips are connected mutually as shown in e.g. fig. 4 or 5 and with the substrate 80;134;154 by means of fine wire conductors, e.g. 116, 118, 120 or alternatively 110, 112 and 114 which are bonded to respective leads e.g. 106, 108 carried by a principal mounting surface 80 (fig. 3).

As is the case of the present invention, the Takiar patent discloses quite correctly an arrangement of chips in a stacked staggered structure, but resorts wholly to a wire bonding technique for connecting the chips mutually or e.g. to leads 106, 108 on a mounting surface which perhaps could be equated with a substrate in the present invention. Moreover, the circuit element appears as monolithic integrated chips (e.g. "semiconductor die" 22 in fig. 2). It is quite evident from the description, claims and figures of the present invention that the interlayer edge connectors of the present invention is not based on wiring, but are formed directly on the exposed portions of the staggered circuit structure and contacting contact pads thereon. Moreover, the present invention is mainly based on thin-film technology and this is, of course, not the case of the Takiar patent.

Certainly it is known in prior art to provide volumetric devices by stacking circuit chips and to some degree also staggering, as disclosed in the Takiar patent which shows a staggered stack of circuit elements as seen to advantage for instance in figs. 3, 4 and 5 thereof. However, the arrangement in the Takiar patent is based on wire-bonding techniques as would be expected when the stacking of integrated circuit chip modules is attempted and for obvious reasons. As will be seen the Takiar patent does not disclose edge connectors and does not even anticipate or suggest the use thereof and for very obvious reasons,

since the deposition of edge connectors in form of current paths provided directly on edge surfaces would require additional pattern steps to be carried out after the actual mounting on the circuit chips itself and this could entail considerable practical problems. On the other hand there have been no practical solutions for depositing current paths directly on the exposed portion of the staggered area in a staggered circuit structure and carried over the edge and down to underlying layers and so on, possibly all the way down to a substrate. This can more easily be realized in a thin-film technology where the step height to be negotiated does not provide an insurmountable obstacle to the use of photolithographic patterning, as explained in the present invention and moreover can be configured geometrically to further obviate any problems involved with conventional photolithographic patterning where depth of field also is a limiting factor. However, this cannot be applicable to conventional stacked circuit chip modules as otherwise known in integrated circuit technology and this is amply underscored by the prior art resorting to either wire bonding or ribbon bonding.

Based on the foregoing amendments and remarks, it is respectfully submitted that the claims in the present application, as they now stand, patentably distinguish over the references cited and applied by the Examiner and are, therefore, in condition for

allowance. A Notice of Allowance is in order, and such favorable action and reconsideration are respectfully requested.

However, if after reviewing the above amendments and remarks, the Examiner has any questions or comments, he is cordially invited to contact the undersigned attorneys.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please amend claims 1-7 as follows:

1. (Amended) A memory and/or data processing device ~~having~~ comprising

at least two stacked layers ~~that overlap~~ overlapping each other partially or completely, ~~wherein~~ said layers ~~are~~ being supported by a substrate or alternatively forming a sandwiched self-supporting structure of ~~such~~ the stacked layers, and ~~wherein~~ at least two layers in the stack ~~comprise~~ including memory and/or processing circuitry ~~that connects~~ connecting electrically to memory and/or processing circuitry in at least one other layer and/or said substrate, ~~characterized in that~~ said layers ~~are~~ being arranged in relation to each other such that contiguous layers form a staggered structure on at least one edge of said device, the edge of at least two layers in said staggered structure forming a set of angular or sloped steps where each step has a height corresponding to ~~the~~ a thickness of each layer, and ~~that~~ at least one electrical edge conductor ~~is~~ being provided passing over the edge of one layer

and down one step at a time enabling ~~the~~ connection to an electrical conductor in any of the layers following in the staggered structure.

2. (Amended) ~~A~~ The memory and/or data processing device according to claim 1, ~~characterized in that~~ wherein said at least one electrical conductor is provided passing over the edge of said staggered structure and connecting electrically to in-layer conductors in two or more and up to a plurality of contiguous layers, negotiating one step at a time.

3. (Amended) ~~A~~ The memory and/or data processing device according to claim 2, ~~characterized in that~~ wherein said in-layer conductors form electrical connections between electrical conductors negotiating the step up to the contiguous layer above and/or down to the contiguous layer below.

4. (Amended) A method for manufacturing a memory and/or data processing device having at least two stacked layers ~~that overlap~~ overlapping each other partially or completely, ~~wherein~~ said layers ~~are~~ being supported by a substrate or alternatively forming a sandwiched self-supporting structure of such stacked layers, and ~~wherein~~ at least two layers in the stack comprise memory and/or processing circuitry ~~that connects~~ connecting

electrically to memory and/or processing circuitry in at least one other layer and/or substrate, and ~~wherein~~ the method ~~is characterized by~~ comprising the steps ~~for~~ of

adding said layers successively, one layer at a time such that the layers form a staggered structure, and ~~for~~

providing one or more layers with at least one electrical contacting pad for linking to one or more interlayer edge connectors.

5. (Amended) ~~A~~ The method according to claim 4, ~~characterized by~~ further comprising providing said layers on a supporting substrate, and forming said staggered structure as a step pyramid.

6. (Amended) ~~A~~ The method according to claim 4, ~~characterized by~~ further comprising providing said layers on a supporting substrate and forming said staggered structure as an inverted pyramid, each of said layers connecting to said substrate via said electrical edge connectors negotiating a single step.

7. (Amended) ~~A~~ The method according to claim 4, ~~characterized by~~ further comprising forming said edge connectors in a process selected ~~among~~ from one of ~~the following, viz.~~ lithography, dry etching, inkjet printing, silk screen printing,

soft lithography, electrolysis, electrostatic deposition~~, or~~ and in situ conversion.